Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled).

2. (Currently Amended) The semiconductor circuit ~~of claim 1 and further~~ comprising:

an image sensor, the image sensor comprising,

a reset transistor having a drain region, a source region, and a gate connected to receive a plurality of reset pulses;

a photodiode connected to the reset transistor; and

a non-volatile memory device connected to the reset transistor and the photodiode.

3. (Currently Amended) The semiconductor circuit of claim 2, ~~wherein~~ the non-volatile memory device further comprising ~~has a drain region, a source region,~~ a floating gate~~, and a control gate that is connected to~~ coupled between the reset transistor and the photodiode.

4. (Original) The semiconductor circuit of claim 3 wherein the plurality of reset pulses occur during a single image capture cycle.

5. (Currently Amended) A semiconductor circuit comprising:

a reset transistor having a drain region, a source region, and a gate connected to receive a plurality of reset pulses;

a photodiode connected to the reset transistor; and

a non-volatile memory device connected to the reset transistor and the photodiode; wherein the non-volatile memory device has a drain region, a source region, a floating gate, and a control gate that is connected to the reset transistor and the photodiode, wherein the plurality of reset pulses occur during a single image capture cycle and ~~The semiconductor circuit of claim 4~~ wherein when a first number of photons are collected by the photodiode, a first number of

electrons are injected onto the floating gate, and when a second number of photons less than the first number are collected by the photodiode, a second number of electrons are injected onto the floating gate that is greater than the first number.

6. (Original) The semiconductor circuit of claim 5 wherein the drain and source regions of the non-volatile memory device have a p conductivity type.

7. (Original) The semiconductor circuit of claim 5 wherein the drain and source regions of the non-volatile memory device have an n conductivity type.

8. (Original) The semiconductor circuit of claim 4 wherein the drain and source regions of the non-volatile memory device have a first conductivity type, and are formed in a semiconductor material of a second conductivity type, the photodiode having a region of the first conductivity type and a region of the second conductivity type, the region of the first conductivity type of the photodiode contacting the control gate of the non-volatile memory device.

9. (Original) The semiconductor circuit of claim 8 wherein the drain and source regions of the non-volatile memory device have a p conductivity type.

10. (Original) The semiconductor circuit of claim 8 wherein the drain and source regions of the non-volatile memory device have an n conductivity type.

11. (Currently Amended) A semiconductor circuit comprising:

a reset transistor having a drain region, a source region, and a gate connected to receive a plurality of reset pulses;

a photodiode connected to the reset transistor; and

a non-volatile memory device connected to the reset transistor and the photodiode; wherein the non-volatile memory device has a drain region, a source region, a floating gate, and a control gate that is connected to the reset transistor and the photodiode, wherein the plurality of reset pulses occur during a single image capture cycle and ~~The semiconductor circuit of claim 4~~ wherein when a first number of photons are collected by the photodiode, a first number of electrons are injected onto the floating gate, and when a second number of photons less than the first number are collected by the photodiode, a second number of electrons are injected onto the floating gate that is less than the first number.

12. (Currently Amended) A semiconductor circuit comprising:

a reset transistor having a drain region, a source region, and a gate connected to receive a plurality of reset pulses;

a photodiode connected to the reset transistor; and

a non-volatile memory device connected to the reset transistor and the photodiode; wherein the non-volatile memory device has a drain region, a source region, a floating gate, and a control gate that is connected to the reset transistor and the photodiode, wherein the plurality of reset pulses occur during a single image capture cycle and wherein when a first number of photons are collected by the photodiode, a first number of electrons are injected onto the floating gate, and when a second number of photons less than the first number are collected by the photodiode, a second number of electrons are injected onto the floating gate that is less than the first number ~~The semiconductor circuit of claim 11~~ and wherein the drain and source regions of the non-volatile memory device have a p conductivity type.

13. (Currently Amended) A semiconductor circuit comprising:

a reset transistor having a drain region, a source region, and a gate connected to receive a plurality of reset pulses;

a photodiode connected to the reset transistor; and

a non-volatile memory device connected to the reset transistor and the photodiode; wherein the non-volatile memory device has a drain region, a source region, a floating gate, and a control gate that is connected to the reset

transistor and the photodiode, wherein the plurality of reset pulses occur during a single image capture cycle and wherein when a first number of photons are collected by the photodiode, a first number of electrons are injected onto the floating gate, and when a second number of photons less than the first number are collected by the photodiode, a second number of electrons are injected onto the floating gate that is less than the first number ~~The semiconductor circuit of claim 11~~ and wherein the drain and source regions of the non-volatile memory device have an n conductivity type.

14. (Original) A method of capturing an image with an imaging cell, the imaging cell comprising:

a reset transistor having a drain region, a source region, and a gate connected to receive a plurality of reset pulses; and

a photodiode connected to the reset transistor,

the method comprising the steps of:

placing a reset voltage on the photodiode by pulsing on the reset transistor; and

collecting photons for a second period of time, the collected photons changing a magnitude of the reset voltage over the second period of time.

15. (Original) The method of claim 14 and further comprising the step of storing a charge that represents a number of photo-generated charge carriers that were collected during the second period of time.

16. (Original) The method of claim 15 and further comprising the step of repeating the placing, collecting, and storing steps a plurality of times to generate a total stored charge.

17. (Original) The method of claim 16 wherein the total stored charge represents a single bit of an image.

18. (Original) The method of claim 16 and further comprising the step of reading the total stored charge to generate a post image cycle current.

19. (Original) The method of claim 18 and further comprising the step of generating a pre-image cycle current prior to collecting photons for the second period of time.

20. (Original) The method of claim 19 and further comprising the step of subtracting the post image cycle current from the pre-image cycle current.